

REMARKS

Claims 1-7 remain pending in the application.

Claims 1-7 over Weng

In the Office Action, claims 1-7 were rejected under 35 USC 102(b) as allegedly being anticipated by U.S. Pat. No. 5,659,698 to Weng et al. ("Weng"). The Applicants respectfully traverse the rejection.

Claims 1 and 2 recite a single coder/decoder having a digital/analog conversion channel time division multiplexed among, and an analog/digital conversion channel concurrently coupled to, a plurality of processors. Claims 3-7 recite 3 means for time division multiplexing a first plurality of processors to a digital signal input of a single coder/decoder.

Weng teaches a circular buffer (Weng, title).

The Examiner cites primarily Fig. 3 of Weng, and col. 11, for allegedly disclosing the multiple processor aspect of the present invention. Fig. 3 shows **ONLY ONE, central** processing unit 58 in communication with a signal converter 56. Fig. 3 fails to show a **plurality** of processors connected to a **single** coder/decoder, much less **multiplexed** as claimed.

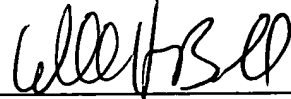
Moreover, the cited col. 11, lines 10-13 of Weng indicates that the auxiliary interface 152 of Fig. 4 can be a serial port with a built in time division multiplexing framing structure. The cited auxiliary interface 152 is shown receiving audio from **ONLY ONE** processor 134, as well as outputting to only one processor 140. Weng fails to disclose a **plurality** of processors connected to a **single** coder/decoder, much less **multiplexed** as claimed.

For at least all the above reasons, claims 1-7 are patentable over the prior art of record. It is therefore respectfully requested that the rejections be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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